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(12) UK Patent Application (19) GB (11) 2 337 633 (13) A

(43) Date of A Publication 24.11.1999

(21) Application No 9810797.2

(22) Date of Filing 20.05.1998

(51) INT CL[6]
H01L 21/82

(52) UK CL (Edition Q)
H1K KFLS K1CA K1FL K4C14 K4H1B K4H1C K4H2 K4H3X

(56) Documents Cited
EP 0337436 A2 US 5247196 A

(58) Field of Search
UK CL (Edition P) H1K KFLS KGAMS
INT CL[6] H01L
ON LINE,W.P.I.

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(54) Abstract Title
Forming capacitors for semiconductor devices

(57) A method of forming capacitors in a semiconductor device, involves providing a first insulating layer 3, providing a first mask with an array of apertures over the insulating layer and etching an array of holes in the first insulating layer through said apertures in the mask. A first electrode layer 7 extending into the holes is formed over the first insulating layer. A dielectric layer 8 extends into the holes on the first electrode layer. A second electrode layer 9 extends into the holes on the dielectric layer. The capacitors are patterned with a second mask. The capacitors can be subsequently connected into the circuit in a sequence of processing steps that only involve the addition of two extra masks beyond those conventionally employed in integrated circuit manufacture.

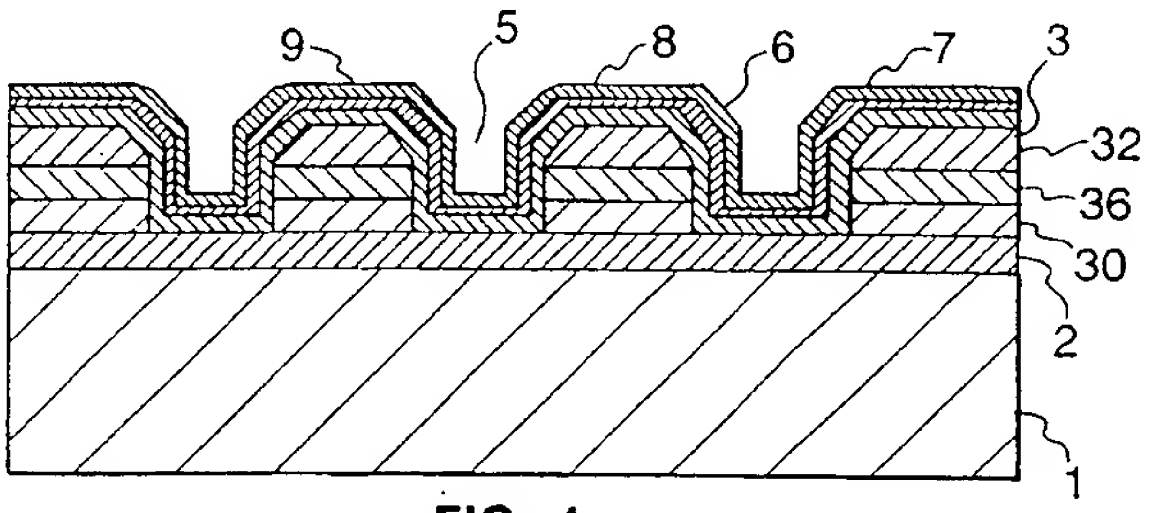

FIG. 1

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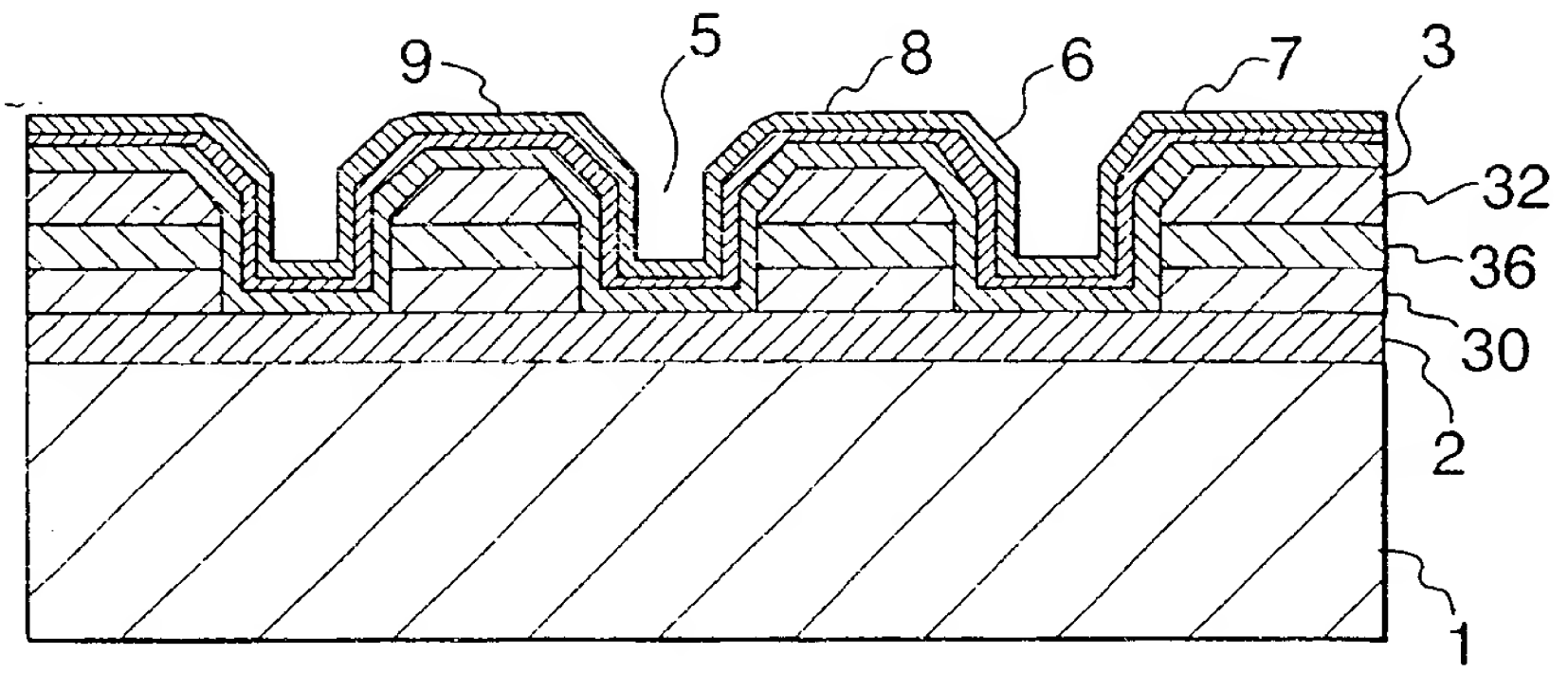

FIG. 1

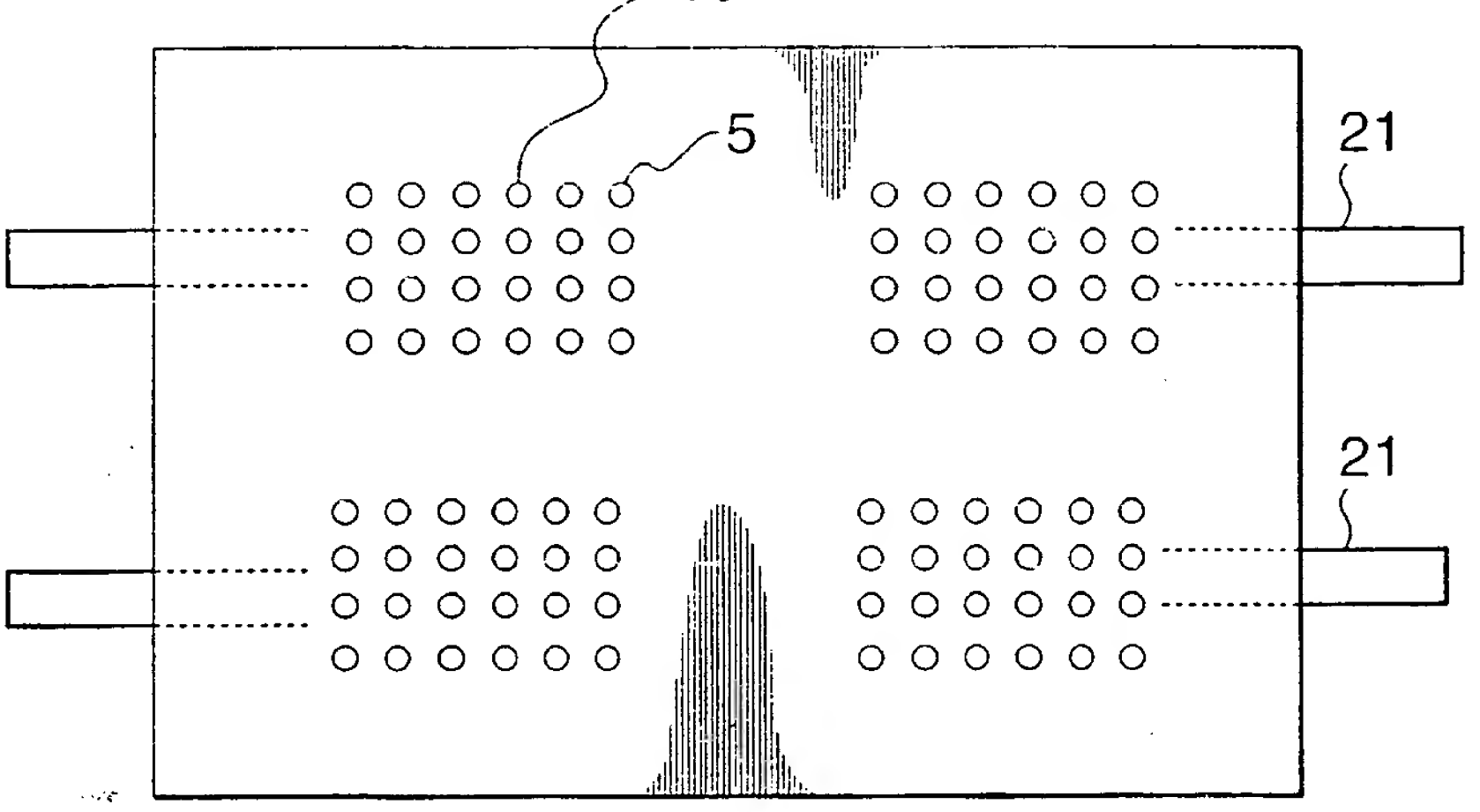

FIG. 2

a first mask with an array of apertures over said insulating layer; etching an array of holes in said first insulating layer through said apertures in said first mask; forming a first electrode layer extending into said holes over said first insulating layer; forming a dielectric layer extending into said holes on said first electrode layer; forming a second electrode layer extending into said holes on said dielectric layer; and pattering said capacitors with a second mask.

This sequence permits a complete manufacturing operation, including the connection to other components on the wafer, for example, transistors and the like, to be carried out with only two additional masking steps.

The dielectric layer can be conveniently formed in a separate chamber, for example, as an oxide layer using rapid thermal oxidation at about 700°C for less than one minute, furnace oxidation at 400-500°C for about 30 minutes, plasma enhanced chemical vapor deposition (PECVD) (typically at 200° to 450° for less than about two minutes). It is also possible to use an integrated oxygen plasma, in which case the wafer is placed in a second chamber a metallization tool where it is exposed to about 1% oxygen in argon. This step can be carried out as a preliminary step to the steps described above. By oxidizing in this manner for about 60 seconds, the free titanium can be burned as a seed layer to facilitate oxidation. The difficulties of forming an oxide layer in a vacuum chamber connected to a cryopump can be avoided due to the high dilution of oxygen in argon. Alternatively, chemical oxidation, for example electrochemical oxidation, can be employed.

Preferably the first insulating layer is formed on a conductive layer, such as a polysilicon layer, for establishing contact with said first electrode layer.

The insulating layer in which the holes are formed is typically an SG/PSG/SOG (Silicate Glass/Phosphorus-doped Silicate Glass/Spin-on Glass) sandwich. The PSG typically contains about 4 wt. % of phosphorus. The spin-on glass is preferably an organic spin-on glass containing about 4 wt. % of phosphorus.

The electrode layers can themselves be composite layers, for example TiN/Ti/TiN or Ti/TiN layers. Preferably, the lower layer consists of a Ti/TiN composite layer to make good contact with the underlying polysilicon contact layer. The upper layer is generally thicker, in the order of 2000Å, and is preferably in the form of a TiN/Ti/TiN sandwich. Ti is normally in tensile stress and TiN is normally in compressive stress, so the sandwich can be structured to reduce the stress in the electrode.

A integrated circuit structure can subsequently be formed in a conventional manner.

Although the dielectric layer can conveniently be titanium oxide, other dielectric layers, such as silicon nitride (Si_3N_4) can be used alone or in combination with the titanium dioxide layer. The silicon nitride layer can, for example, be deposited by PECVD (plasma enhanced chemical vapor deposition).

The invention will now be described in more detail, by way of example only, with reference to the accompanying drawings, in which:-

Figure 1 is a schematic cross-sectional view of a semiconductor device with a capacitor formed thereon;

Figure 2 is a plan view of a portion of a wafer having capacitors formed thereon;

Figures 3 to 7 illustrate the various processing steps involved in fabricating capacitors in accordance with the invention; and

Figure 8 shows an alternative embodiment.

In Figure 1, a silicon substrate 1 has various components, such as transistors and the like (not shown) formed therein by previous process steps known in the art. In order to provide high value capacitors 10 in the device, a layer of polysilicon 2 is first deposited on the surface of the wafer and patterned to provide a contact for the bottom electrode for the capacitor 10.

Next a composite layer 3 is deposited by conventional means onto the polysilicon layer 2. The insulating layer 3 typically consists of a lower layer of silicate glass, an intermediate layer of phosphorus-doped silicate glass (containing 4 wt. % P), and an upper layer of inorganic spin-on glass (also containing 4 wt. % P). The formation of such an insulating layer is conventional and well understood to a person skilled in the art. Layer 3 typically has a total nominal thickness of 0.8 micron.

After application of a first extra mask (not shown), a series of arrays of holes 5 are etched in the insulating layer 3. Each array will form a capacitor in a manner to be described. This mask is referred to as an extra mask because it involves a masking step over and above what would normally be required in conventional integrated circuit processing.

After bevelling the corners 6, for example, by carrying out an isotropic etch or an integrated sputter etch, a lower electrode 7 is sputtered onto the insulating layer 3 in a

sputtering chamber initially in the presence of an inert gas, such as argon. The lower electrode layer 7 consists of a titanium layer followed by a titanium nitride layer. The lower Ti sublayer is preferred in order to make a good electrical contact with the underlying polysilicon layer 2. The titanium nitride layer can be deposited by changing the inert gas in the sputtering chamber to nitrogen. This electrode layer 7 typically has a total thickness of 0.01 to 0.1 microns.

Next the wafer is moved to a different system where a titanium oxide (TiO_2) layer 8 is formed, typically by thermal oxidation at 400 – 500°C for less than about thirty seconds (or by plasma oxidation at about 200°C for about 2 mins) on the titanium nitride sublayer. Alternatively, the oxide layer can be formed by rapid thermal oxidation (RTO) at 700°C for about 1 minute. This oxide layer typically has a thickness of 50 to 1000 Angstroms.

As a preliminary step the free titanium can be oxidized *in situ* in the metallization tool. In that case, the wafer is transferred to a second chamber where it is placed in 1% of oxygen in argon plasma for about one minute. This creates a seed oxidation layer from the free titanium, which enhances subsequent oxidation.

Finally, the wafer is returned to the sputtering chamber, and the upper electrode layer 9, consisting of a TiN or preferably a TiN Ti/TiN sandwich is deposited. This upper layer 9 has a thickness of about 0.01 to 0.1 microns.

Since the dielectric layer 8 is deposited in a separate system, other suitable dielectrics can be employed, for example, silicon nitride (Si_3N_4), although this does not have as good dielectric properties as TiO_2. Another possibility is to employ a combination of TiO_2 and (Si_3N_4).

Figure 3 shows the wafer prior to the formation of the capacitors 10. The device has a field oxide layer 20 in the silicon substrate 1 and a transistor 25 having source 21, drain 22, gate oxide 23, and gate 24. The gate 24 is a polysilicon layer that is deposited with the contacts 2 as a common layer which is then patterned to make the bottom electrode contacts 2 and the gate electrodes 24.

The SG/PSG/SOG layer 3 is then deposited as shown in Figure 4 and the capacitors 10 formed as described with reference to Figure 1.

After formation of the capacitors 10, the capacitor layers 7, 8, 9 of course extend across the whole wafer. The next step is to pattern the individual capacitors. As this step

requires an additional mask over and above that normally used, this is considered a second extra masking step. A conventional mask can be employed.

Once formed, the capacitors 10 have been patterned, an isolation oxide layer 30 is applied across the whole wafer to give a structure as shown in Figure 4. The isolation oxide layer is applied by PECVD to isolate the individual capacitors 10. This isolation layer is necessary to ensure that the edge 10' of the layers 7, 8, 9, of the capacitors 10 are protected against shorts when subsequent metal interconnect layers 41 are applied.

The next step is to mask the isolation layer 30 and etch holes 40 through the dielectric 3 to reach to the source, drain and gate regions of the transistors 1. This step is conventional. Subsequently, metal interconnect layer 41 (typically an aluminum alloy with a TiN anti-reflective coating) is applied onto isolation layer 30. The interconnect layer 41 (M_1 layer) extends into the holes 40 to establish contact with the source 21, drain 22, and gate 24 of the transistors 25. Contact to the electrodes of the capacitors is not yet established because the etching of the contact holes 40 would cause the penetration and complete etching of the upper electrode layer 9 of the capacitors because over-etching would occur due to the fact that the oxide layer 3 is at least ten times thicker over the transistors 25 than over the capacitors 10, resulting in a local destruction of the capacitors.

After patterning the layer 41 (M_1 layer), a further insulation layer 50 is applied as shown in Figure 7. This layer consists of a conventional $ID_1/SOG/ID_2$ layer, where ID stands for interlayer dielectric. ID is typically SRSG (silicon rich silicon glass) and the SOG in this case is typically a semi-organic spin-on glass.

After applying insulation layer 50, a mask (not shown) is applied and via holes 51 are etched through the layer 50 to the upper electrode 9 of isolating the capacitors 10 and to the layer 41 where it is desired to establish interconnections. This is a standard procedure. Subsequently, a second aluminum interconnect layer 52 (M_2 layer) is applied over the layer 51. The M_2 layer is used in conventional i.c. processing to establish connections to the M_1 layer, and in this case is used additional to establish connection with the upper electrodes 9 of the capacitors. The layer 52 is subsequently patterned in a conventional manner.

Since the M_1 layer 41 is generally much thicker than the upper electrode layer 9, there is no risk of over-etching because the via holes 51 reach the interconnect layer 41 before they reach the thinner electrode layer 9. Etching can be terminated as soon as

the holes reach electrode layer 9. There is thus no risk of an over-etch causing destruction of the capacitors, yet contact with both the electrode layer 9 and the interconnect layer 41 is assured.

Figure 8 shows an alternative embodiment, where conventional capacitors 60 are formed prior to making the conformal capacitors 10 and then connected in parallel. In conventional i.c. technology, capacitors 60 are formed by first providing an additional poly layer 61 under the poly layer 2. A dielectric layer 62 is formed between the two poly layers 2, 61. In accordance with the invention, additional capacitors 10 can be formed on top of the conventional capacitors in a manner described above. The capacitors 10 and 60 are connected in parallel to create a composite capacitor having a capacitance equal to the sum of the two individual capacitances.

Figure 2 is a plan view of a portion of a wafer showing the capacitors 10 consisting of arrays of holes 5. Connection to the lower poly layers 2 is by means of connections 2'. The holes typically have a diameter and spacing of about 1 micron.

The described method permits high value capacitors to be formed in an economic manner with only two additional masking steps. The only extra masking steps required are the first extra mask to form the holes 5 and the second extra mask to pattern the capacitors. Extra deposition steps are required to form the capacitors, but the remaining connections are made using standard processing steps. The method is particularly suitable for working a 0.8 micron line widths and below. Also, the capacitors have metal electrodes, which lead to extremely good voltage coefficients.

Claims:

1. A method of forming capacitors in a semiconductor device, comprising the steps of:

a) providing a first insulating layer on a wafer;

b) providing a first mask with an array of apertures over said insulating layer;

c) etching an array of holes in said first insulating layer through said apertures in said first mask;

d) forming a first electrode layer extending into said holes over said first insulating layer;

e) forming a dielectric layer extending into said holes on said first electrode layer;

f) forming a second electrode layer extending into said holes on said dielectric layer; and

g) pattering said capacitors with a second mask.

2. A method as claimed in claim 1, wherein an isolation layer is deposited on said wafer over said second electrode layer to isolate the edges of said first and second electrode layers.

3. A method as claimed in claim 2, wherein said dielectric layer is formed in a separate chamber.

4. A method as claimed in claim 3, wherein said dielectric layer is formed by furnace oxidation.

5. A method as claimed in claim 4, wherein said dielectric layer is formed by plasma oxidation.

6. A method as claimed in claim 4, wherein said dielectric layer is formed by rapid thermal oxidation.

7. A method as claimed in any one of claims 4 to 6, wherein an initial seed layer is formed by partial oxidation of the second electrode using an integrated oxygen plasma.

8. A method as claimed in any one of claims 2 to 6, wherein after forming said isolation layer, holes are etched through said first insulating layer to active components in the wafer, a first metal layer is applied to said first insulating layer to contact said active components, a second insulating layer is applied over said first metal layer, via holes are etched through said second insulating layer to said second electrode layer of

said capacitors, and a second metal layer is applied to contact said second electrodes through said via holes.

9. A method as claimed in claim 8, wherein said first and second metal layers are patterned after deposition.

10. A method as claimed in any one of claims 1 to 9, wherein said first insulating layer is a composite layer.

11. A method as claimed in any one of claims 1 to 9, wherein said composite layer comprises SG/PSG/SOG.

12. A method as claimed in claims 11, wherein said PSG contains about 4 wt. % of phosphorus and said SOG is an inorganic SOG containing about 4 wt. % of phosphorus.

13. A method as claimed in any one of claims 1 to 12, wherein said first electrode layer comprises a Ti/TiN composite layer.

14. A method as claimed in any one of claims 1 to 13, wherein said second electrode layer comprises a TiN/Ti/TiN composite layer.

15. A method as claimed in any one of claims 1 to 14, wherein said dielectric layer is titanium oxide.

16. A method as claimed in any one of claims 1 to 14, wherein said dielectric layer is silicon nitride.

17. A method as claimed in any one of claims 1 to 14, wherein said dielectric layer is a composite layer comprising a titanium oxide sublayer and a silicon nitride sublayer.

18. A method of forming capacitors in a semiconductor device, substantially as hereinbefore described with reference to the accompanying drawings.

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Application No: GB 9810797.2 **Examiner:** C.D.Stone
Claims searched: All **Date of search:** 4 August 1998

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.P): H1K(KFLS,KGAMS)

Int Cl (Ed.6): H01L

Other: ON LINE,W.P.I.

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	EP 0337436 A2	NEC	1
X	US 5247196	MITSUBISHI DENKI	1

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.